REMARKS

This REQUEST FOR RECONSIDERATION UNDER 37 CFR 1.116 is filed in reply to the outstanding Office Action of November 19, 2003, and is believed to be fully responsive thereto and to place this case in condition for allowance for reasons set forth below in greater detail.

Reconsideration is respectfully requested of the rejection of claims 1, 3-10 and 12-21 under 35 USC 103(a) as being unpatentable over Leung, particularly in view of the following comments on the very major distinctions of the present invention over Leung and why one skilled in the art would never ever consider attempting to modify Leung in a manner as suggested in the prior art rejection to achieve the circuit architecture and designs of the present invention.

The present Final Rejection essentially repeats the previous prior art rejection. However, the explanation from page 3, line 1, to page 4, line 4 (a third data bus...access to the shared bus.) is new, and the Response to Arguments on page 6 is also new, and is not believed to be technically correct.

The Examiner states in the Response to Arguments that "Regarding Applicant's argument that Leung teaches simultaneous read and write operations using dual ports, the Examiner disagrees. Leung teaches simultaneous reading and writing operations by reading and writing the read register and the write register in parallel and not by simultaneously accessing the cache."

This is believed to be technically incorrect. Refer to column 3, lines 12-21, which state, "The control circuit includes an SRAM cache, which has the same configuration as each of the memory banks. A cache read buffer is coupled between an output port of the SRAM cache and the write buffer, thereby facilitating the transfer of data from the SRAM cache to the memory banks. Similarly, a cache write buffer is coupled between an input port of the SRAM cache and the read buffer, thereby facilitating the transfer of data from the memory banks to the SRAM cache."

Note also that Read-Write port 313 in Figure 5 has an input line and an output line, while Write only port 312 has only an input line. Similarly Read buffer 171 in Figure 1 has only an output line, and Write buffer 172 has only an input line.

Leung Compared To The Invention

The present invention provides a high speed embedded single port DRAM having an interface circuit for operation with a single port SRAM cache memory which has a completely different architecture and operating scheme than the dual port DRAM/dual port SRAM of the reference Leung. The dual port DRAM/dual port SRAM of Leung is approximately 3 times larger than the single port DRAM/single port SRAM of the present invention, and is designed for completely different purposes and to operate in a completely different manner from the present invention.

The present invention provides an embedded DRAM having an interface circuit for a single port SRAM wherein the single port in the SRAM cache memory is time shared for read and write operations, and at any one time can perform only a read operation or a write operation. The embedded DRAM is only approximately 1/3 the size of the DRAM of Leung. In

the present invention, the bi-directional data bus 1 and the MUX 200 allow the single port in the SRAM cache 100 to be used in either a read operation or a write operation. The shared single port SRAM is also the reason why the present invention implements the pipeline operations with the least number of cycles as illustrated in Figures 2-5, having the pipeline sequences of operation of Figure 7, and as specified by claims 11-21. The dual port DRAM/dual port SRAM of Leung operates in a completely different manner and has no need for any of these details.

The dual port DRAM/dual port SRAM of Leung has a first write only port and a second read/write port (as specified by claim 3 of Leung for example) which can perform both read and write operations. The dual ports of the DRAM and the dual ports of the SRAM of Leung enable the DRAM/SRAM to perform simultaneous read and write operations, and allow the major object of Leung which is to perform hidden memory refresh operations at any time without interfering with normal operations of the DRAM. See the FIELD OF THE INVENTION in column 1 and the SUMMARY in columns 2-5.

Column 8, lines 52-56, of Leung describe "perform a read operation and a write operation during the same cycle of the CLK signal", which according to one of the present inventors Louis Hsu requires and means a dual port SRAM. The next sentence then states "using dual-port SRAM cells, which can be used to support read and write operations during a single cycle of the CLK signal". These sentences are somewhat confusing, and "the same cycle" and "a single cycle" are equivalents, but both operating modes and embodiments as described therein would require dual ports to support the described operations according to one of the present inventors Louis Hsu who is very knowledgeable in this technical field.

Accordingly, the dual port and dual unidirectional bus architecture of Leung is required to perform the major objects and functions of Leung, which are completely different from the major objects of the present invention, as specified in the SUMMARY of the present patent application on pages 1-2. The major objects and functions of Leung are also the reasons why one skilled in the art would never ever consider modifying Leung for operation similar to the present invention with a DRAM having a single port SRAM cache memory, and a bi-directional data bus operating through a MUX to the single port. This is primarily because a circuit designed to operate in that manner would not fulfill the major objects of Leung, which are to perform hidden memory refresh operations at any time and in a way that the refresh operations do not interfere with external access operations (see Leung, FIELD OF INVENTION).

The design objective of Leung is basically to hide a data refresh cycle such that it does not interfere with external access operations, whereas the design objective of the present invention is to minimize the cycle time to access data over very wide data buses, which are entirely different design objectives which result in entirely different architectures.

A key difference between the cache interface architecture design (more specially the data path design) of the present invention and other prior art designs is that the present invention minimizes the number of clock cycles for either read or write operations, including both hit and miss situations. This has not even been discussed in any of the prior art.

In order to fulfill this objective, the present invention has (1) the bi-directional 512 data path at the neck region and a MUX 200, (2) a write buffer 500 directly connected between DQ and Write register 400, (3) a MUX 700 taking inputs either from Read Register 300 or Write register 400 to a read buffer 600 to send them to DQ.

Figure 5 explains clearly the data flow in a write miss case. No known prior art data interface will facilitate such a write miss data transfer in a pipe-line fashion.

Write miss is defined, in the cache 100, when it is desired to write a word line of data in the cache which is 512 bits wide from the external DQ, but the operation only requires to write 1/4 of it, in other words, the other 3/4 is from the eDRAM. At this point the 512 bits from eDRAM is loaded to 900 Write Buffer, and 64 bits of new data is loaded to WB 500, and both of them are mapped to Write Register 400, the 64 bits of the new data will overwrite the 64 bits of the old 512 bit data, and the whole modified 512 bits data will be sent to Cache 100 through MUX 200. At the same time, the old 512 bits of data from the Cache 100 are retired from Cache 100 back to eDRAM.

This type of write miss operation is entirely novel relative to the prior art and Leung.

The architecture of the present invention, with the very wide data buses, uses pipe-line operations. Referring to Figure 1 of this application, the very wide bi-directional data bus 1, connecting the SRAM cache 100 through MUX 200 to either read register 300 or write register 400, will not support simultaneous read and write operations.

The described architecture of Leung does support simultaneous read and write operations, and so Leung does not have a similar bi-directional data bus, but must instead use two separate unidirectional data buses, and the use of a single bi-directional data bus would defeat the major purpose of Leung as noted above. Column 8, lines 3-7, state "Dedicated read bus DB[255:0] and dedicated write bus DA[255:0] are employed, so that one of DRAM banks 0-

63 can perform a write operation while another one of DRAM banks 0-63 can perform a read operation simultaneously."

The simultaneous read and write operations described by Leung require two separate data buses, rather than a single very wide bi-directional data bus and MUX (as specified by claim 3).

Moreover, the very different design objectives of Leung as described above would not make the single bi-directional data bus arrangement (with the MUX of claim 3) of the present invention at all obvious over Leung.

Additionally, the architecture of Leung will not support the novel write miss operation described above.

Moreover, the applicant has the following additional comments on the written reasons for the prior art rejection on pages 2-6 of the Office Action. Those written reasons gloss over the many distinctions of the present invention relative to Leung by merely referring to interconnected components such as the DRAM, the SRAM cache 188, read buffer 188, and write buffer 189. When the claims specify particular data buses, such as the second through eleventh data buses, the prior art rejections gloss over the particular recitations and merely refer broadly to the connections between the components.

This application is now believed to be in condition for allowance, a Notice of Allowance is respectfully requested. If the Examiner believes a telephone conference might expedite prosecution of this case, it is respectfully requested that he call applicant's attorney at (516) 742-4343.

Respectfully submitted,

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